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10/057,393	01/25/2002	Brian Hoang	5500-74100	1596

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EXAMINER	
WONG, WARNER	
ART UNIT	**PAPER NUMBER**
2668	

DATE MAILED: 11/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/057,393	HOANG, BRIAN	
	Examiner	Art Unit	
	Warner Wong	2668	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-16* is/are allowed.

6)☒ Claim(s) *1-10 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Clauburg (6,689,018).

Regarding claim 1, Clauburg describes an ATM apparatus (digital system) comprising:

a plurality of units (fig. 3C, 14.1/15.1 pair – 14.5/15.5 pair) operating at a first clock rate, each unit configured to independently process a sequence of data items (fig. 3C, where data items/cells A, B, etc. from input stream #30 are processed by processing unit pairs along paths #13.1-13.5, and each path "clocks in" the cells only at a particular time frame 't0+xT', col. 3, lines 39-56).

a domain crossover element (fig. 3C, demux #12) configured to receive a stream of data items(fig. 3C, #30) at a second clock rate (for every 't', col. 3, lines 43-56) and configured to distribute separate sequences of data items through separate ports (paths) to the plurality of units (fig. 3C, 14.1/15.1 pair – 14.5/15.5 pair).

Regarding claim 2, Clauburg describes all claim limitations set forth in claim 1. Clauburg further describes the second clock rate being greater than the first clock rate (col. 3, lines 43-45, where the the rate of every 't' > rate of 't0+xT') and the number of ports (paths) equals a positive integer multiple of the ratio of the second clock rate to the first clock rate (col. 3, lines 26-29, where each of the 5 processing paths has a "clock in" rate equaling 1/5 to that of the input stream).

Regarding claim 3, Clauburg describes all claim limitations set forth in claim 2. Clauburg further describes that the number (N) for de-multiplexing [i.e. # de-mux output ports] may be 2 (col. 3, lines 20-21, with N=1,2,3..)

Regarding claim 4, Clauburg describes all claim limitations set forth in claim 1. Clauburg further describes that the units are (general purpose) processors (col. 3, lines 30-31).

Regarding claim 5, Clauburg describes ATM cells (data items/packets), in which each **[inherently]** have a standard ATM cell header comprising of a packetID (Content type), targetID (VCI), Control flags (Access Control Field) plus the packet data (information) (fig. 7.9 of Halsall, "Data Communications, Computer Networks and Open Systems", © 1992, p. 322, is provided as a reference but is not used in the rejection).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clauburg in view of Chung (5,764,895).

Regarding claim 6, Clauburg describes all claim limitations set forth in claim 1.

Clauburg lacks what Chung describes: the domain crossover element (LAN device) includes a circular buffer having a plurality of distinct sections (fig. 5, packet

buffers #112,114, 116,118) each associated with a corresponding one of the separate ports (col. 5, lines 27-34, where each packet in fig. 5's packet buffer corresponds to a transfer between the LANs/ports).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to incorporate the design of circular buffer implementation of Chung into the de-multiplexer of Clauburg. The motivation being that such implementation "provides quick efficient cut-through [between network segments] with zero host processor overhead." (Chung, col. 4, lines 38-40).

Regarding claim 7, Clauburg and Chung combined describe all claim limitations set forth in claim 6.

Chung further describes that the separated sequences of data items (packet, fig. 5, #112,114,116,118) is formed by repeatedly reading from the sequential storage locations a corresponding section of the circular buffer (fig. 5, #122,124,126,128,130).

Regarding claim 8, Clauburg and Chung combined describe all claim limitations set forth in claim 6. Chung further describes that that number of storage locations N is greater than 2 (fig. 5, #122,124,126,128,130).

Regarding claim 9, Clauburg and Chung combined describe all claim limitations set forth in claim 8.

Clauburg and Chung lacks describing that N=4.

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to specify that the number of storage locations N=4, since it has

been held that discovering an optimum value of a result effective variable involves only routine skill in the art (in re Boesch, Eli f.2d 272, 205 USPQ 215).

4. **Claim 10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Clauburg as applied to claim 1 above, and further in view of a 5-stage Johnson counter (whereinafter denoted as "Johnson Counter"), Talarek (6,628,679) and the Segal (4,685,101).

Clauburg describes all claim limitations set forth in claim 1.

Clauburg lacks what a Johnson Counter describes

a counter/decoder (Johnson Counter) that receives an input clock (fig. 6, CP0) and responsively asserts sequential ones of a plurality of output signals (fig. 6, O0-O9 output);

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to specify a Johnson counter as a timing generator/sequencer to latch in individual data items from the input stream within the demultiplexer of Clauburg. The motivation of using (any) timing generator is to provide an accurate interval to "latch" input data to output.

Clauburg and the Johnson Counter combined lack what Talarek describes:

a plurality of storage location registers (fig. 5, #500,520, 560), each coupled to receive corresponding one of the plurality of output signals from the counter, (fig. 5, input clocks A, B, N) and each coupled to receive a stream of input data items (fig. 5, input), wherein each of the storage location registers is configured to store an input data

item when the corresponding one of the plurality of output signals is asserted (col. 5, lines 8-15);

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to design the de-multiplexer of Clauburg as the de-multiplexer of Talarek which uses storage location registers. The motivation being that it alls the data to be latched should the transmitted/incoming data is skewed in phase (Telarek, col. 1, lines 21-24).

Clauburg, the Johnson Counter and Talarek combined lack what the Segal describes:

a plurality of (sub)multiplexers (fig. 1, M12) each configured to provide a sequence of data items to one of the separate ports (fig. 1, M12's DS2 outputs), wherein each of the (sub)multiplexers is coupled to storage location registers (fig. 1, DS1 inputs) associated with said one of the separate ports (fig. 1, DS1 inputs associated with the corresponding [output port of] M12 sub-multiplexer).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to specify, within the demultiplexer described by Clauburg, the Johnson Counter and Talarek, multiple sub-multiplexers each combining a subset of inputs data items into an output sequence. The motivation being that the plurality of units which receive the exclusive output sequences may require such (combined sequence) input format or length.

Clauburg, the Johnson Counter, Talarek and Segal combined lack what the Johnson Counter (further) describes:

an output counter (Johnson Counter) that receives an output clock (fig. 6, CP0), wherein the output counter is coupled to one or more of the (sub)multiplexers (fig. 6, via outputs O1-O9) and configured to sequentially select (pulse/latch out) storage locations for the one or more (sub)multiplexers to access to provide said sequences of data items (to generate DS2 in Segal).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to specify a Johnson counter as a timing generator/sequencer to latch out a sequence of data items from the M12 (sub)multiplexer of Clauburg, the Johnson Counter, Talarek and Segal. The motivation of using (any) timing generator is to provide an accurate interval to "latch" input data to output.

5. Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clauburg in view of Talarek and Segal.

Regarding claim 17, Clauburg describes a demultiplexer (method) (fig. 3C, #12) of distributing a stream of data items received at a first clock rate (for every 't', col. 3, lines 43-56) among a plurality of processing units (fig. 3C, 14.1/15.1 pair – 14.5/15.5 pair) operating at a second, slower clock rate (col. 3, lines 26-29, where each of the 5 processing paths has a "clock in" rate equaling 1/5 to that of the input stream).

Clauburg lack what Talarek describes:

sequentially selecting one of a plurality of registers (fig. 5, #500,520, 560) at the first clock rate (fig. 5, via input clocks A,B,..N, which have input data streams' clock rates);

storing each data item from the stream of data items in a selected register as the data items are received (fig. 5, #500,520, 560).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to design the de-multiplexer of Clauburg as the de-multiplexer of Talarek which uses storage location registers. The motivation being that it alls the data to be latched should the transmitted/incoming data is skewed in phase (Telarek, col. 1, lines 21-24).

Clauburg and Talarek combined lack what the Segal describes:

sequentially selecting (multiplexing, fig. 1, M12) one of the first subset of plurality of registers (fig. 1, corresponding DS1s) at a second clock rate (inherent DS2 speed).

sequentially selecting (multiplexing, fig. 1, M12) one of the first subset of plurality of registers (fig. 1, corresponding DS1s) at a second clock rate (inherent DS2 speed).

concurrently reading data items from the selected ones of the first and second subsets [at the second clock rate] (col. 1, lines 54-58, "As is shown, this is accomplished by providing seven M12 multiplexers, each of which [independently/concurrently] multiplexes four DS1 lines into a single DS2 line.")

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to specify, within the demultiplexer described by Clauburg and Talarek, multiple sub-multiplexers each combining a subset of inputs data items into an output sequence. The motivation being that the units which receive the exclusive output sequences may require such (combined sequence) input format or length.

Regarding claim 18, Clauburg, Talarek and Segal combined describe all limitations in claim 17. Clauburg, Talarek and Segal further describe: (Clauburg, fig. 3A-C) the de-multiplexer output cells at different time, yielding the first data item read from the first subset (Segal, fig. 1, first M12) is read at a different time than the first data item read from the second subset (Segal, fig. 1, second M12).

Regarding claim 19, Clauburg, Talarek and Segal combined describe all limitations in claim 17. Clauburg, Talarek and Segal further describe: all registers in the second subset are written after all registers in the first subset (Clauburg, fig. 3A-C) the de-multiplexer output cells at sequentially [to its internal registers], where the first subset (Segal, fig. 1, first M12) comprises a first batch of cells A & B, the second subset (Segal, fig. 1, second M12) comprises a second batch of cells C, D & E.)

6. **Claim 20** is rejected under 35 U.S.C. 103(a) as being unpatentable over Clauburg in view of Talarek and Segal as applied to claim 17 above, and further in view of Kariquist (2003/0063626).

Clauburg, Talarek and Segal combined describe all limitations in claim 17. Clauburg, Talarek and Segal lack what Kariquist describes:

continuously repeating the acts of claim 17 while a reset (enable) signal is de-asserted (fig. 7, where the enable/reset signal may cut off power to the input mux (device), discontinuing all operations.)

It would have been obvious to one with ordinary skill in the art at the time of invention to deploy a reset (enable) signal to control the operations of (any) device. The

motivation being that if pertinent error condition arises, the reset signal may halt operations of the devices so that the entire system will not be corrupted.

Allowable Subject Matter

7. Claims 11-16 allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Warner Wong whose telephone number is 571-272-8197. The examiner can normally be reached on 5:30AM - 2:00PM, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Warner Wong
Examiner
Art Unit 2668

WW

CHIEH M. FAN
PRIMARY EXAMINER